CALL FOR PAPERS

2018 Summer Simulation Multi-Conference
50th Summer Computer Simulation Conference

Track Chair: *Alberto A. Del Barrio, Universidad Complutense de Madrid, Spain, abarriog@ucm.es*
Co-Chair: *Seda Ogrenci Memik, Northwestern University, IL, seda@eecs.northwestern.edu*

Aims and Scope

This track is specially intended to those works tackling the simulation problem during the entire design flow for electrical circuits. Simulation is an important mechanism to detect errors in the earlier design stages, allowing the designers to correct them and accelerate the time to market of their circuits.

Simulations during the design stage can be mainly classified into three categories: behavioral, structural and post-route, each of them with a different accuracy/runtime tradeoff. It is a major challenge to optimize this relationship either with new models or utilizing hardware platforms to increase the simulation speed without losing or sacrificing very little precision.

In the Internet of Things era, studying the performance of distributed architectures where dynamic events may happen is essential. These unexpected events can range from sensing a value to process variations and aging. Hence, modeling and simulating them is also encouraged.

Furthermore, nowadays the simulation of accelerators based on new arithmetic operators or Machine Learning techniques has also become a hot topic. For instance, the training and validation stages of Neural Networks can be also understood as a modeling and simulation problem, where precision and energy consumption estimations are critical prior to deploying them.

Many of the topic areas involve a deep knowledge about simulation, Design Automation, High-Level Synthesis and in general computer architecture. Modeling, distributed simulations or GPU and FPGA simulating platforms are among the hot-topics of ACM-SIGSIM, and have been heavily promoted at WSC'17 or ACM-SIGSIM PADS.

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Topics

High-quality papers in all aspects of simulation during the Design Automation flow are solicited, including (but not restricted to) the following areas:

- Advanced modeling techniques in High-Level Synthesis, and their execution using novel simulation algorithms.
- Simulation of approximate circuits and novel arithmetic techniques.
- Simulation of hardware-based neural networks.
- Simulation of On-Chip Machine Learning circuits.
- Simulation of Sensor Networks.
- Parallel algorithms and high performance simulation during the synthesis, placement and routing stages.
- GPU, FPGA and hybrid architecture acceleration.
- Simulation based on distributed controllers.
- Process and delay variation modeling and simulation in datapaths.
- Radiation effects simulation in reliable circuits.
- Datapaths based on variable latency blocks simulation.
- Power and energy simulations to evaluate the design automation algorithms.
- Temperature and aging simulations during the design flow.
- MPSoCs and 3D chips simulation during the synthesis, placement and routing stages.
- Simulation during the Design Space Exploration.
- Simulation visualization techniques to help debug designers.

Submission Guidelines

Original, high-quality technical papers are solicited for review, possible presentation and subsequent publication in the conference proceedings. For further instructions, please refer to the Submission Instructions in the SCS Conference Proceedings Management System web site. Contributed papers are 12 pages long with single column format. For author guidelines on how to submit a paper go to: http://scs.org/authorskit/. They will be peer reviewed and – if accepted and presented at the conference - possibly submitted to the ACM and IEEE Digital Libraries. Papers must not have appeared before (or be pending) in a journal or conference with published proceedings, nor may they be under review or submitted to another forum during SummerSim'18 review process. At least one author of an accepted paper must register for the symposium and must present the paper at the symposium.

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Important Dates

Full Paper submission: March 30, 2018
Author Notification: May 4, 2018
Submission of WIP papers: May 11, 2018
Notification of WIP papers: May 18, 2018
Camera-ready Paper: May 25, 2018

Contact

For questions, please contact the track chair, Alberto A. Del Barrio, abarriog@ucm.es or scs@scs.org | (858) 277-3888