



2017 Summer Simulation Multi-Conference (SummerSim 2017)

49th Summer Computer Simulation Conference (SCSC 2017)

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VERIFICATION AND VALIDATION OF COMPUTER SIMULATION MODELS (V&V)

TRACK CHAIRS

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AIMS AND SCOPE

Simulation has been and still remains the predominant means for verification of computer systems. However, simulation cannot guarantee exhaustiveness of the verification. Many semiconductor and intellectual property (IP) design companies have been resistant to adopting formal verification because of the complexity when coming from a simulation-based environment.

In the last 15 years, significant progress was made in both the speed and capacity of Boolean Satisfiability (SAT) solvers that are now at least 5 orders of magnitude faster and can solve formulas that are at least 5 orders of magnitude bigger than before. These advances resulted in corresponding increases in the speed and capacity of formal verification tools. Thus the open research question of how best to integrate these advances in what has traditionally been simulation-only based verification environments.

TOPICS

- Languages for describing systems and properties
- Efficient use of abstraction
- Compositional verification approaches
- Counterexample analysis
- Efficient use of SAT solvers and Satisfiability Modulo Theories (SMT) solvers
- Selection of properties to verify given a simulation model to be verified
- Adopting Artificial Intelligence (AI) approaches to verification of complex systems
- Novel tool flows that integrate formal verification in simulation-based environments
- Case studies

TECHNICAL PROGRAM COMMITTEE

- Flavio M. de Paula (IBM, U.S.A.)
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- Robert Wille (Johannes Kepler University Linz, Austria)
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SUBMISSION GUIDELINES

For the submission guidelines go to <http://scs.org/authorskit/>. Papers should be submitted through the following link: <http://www.softconf.com/sim/SCSC17/>.