



2017 Summer Simulation Multi-Conference (SummerSim 2017)

49th Summer Computer Simulation Conference (SCSC 2017)

July 9 - 12, 2017 | Bellevue, Seattle Suburb, Washington, USA

Simulation in the System Design Flow (SDF '17)

TRACK CHAIRS

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AIMS AND SCOPE

This track is specially intended to those works tackling the simulation problem during the entire design flow for electrical circuits. Simulation is an important mechanism to detect errors in the earlier design stages, allowing the designers to correct them and accelerate the time to market of their circuits.

Simulations during the design stage can be mainly classified into three categories: behavioral, structural and post-route, each of them with a different accuracy/runtime tradeoff. It is a major challenge to optimize this relationship either with new models or utilizing hardware platforms to increase the simulation speed without losing or sacrificing very little precision.

Simulation methods also depend on the selected architecture. Thus, the centralized or distributed nature of the datapath controller determines the model and how to simulate it. Works dealing with unconventional noncentralized architectures are especially encouraged in this track. Another important factor is the presence of dynamic events, such as delay variations or variable latency blocks. Hence, the introduction of external sources of variability or the module libraries, on which the designs are based, are also critical. Conventional simulators use to be static, so simulation engines able to handle with these unexpected events are also encouraged.

Many of the topic areas involve a deep knowledge about simulation, Design Automation, High-Level Synthesis and in general computer architecture. Modeling, distributed simulations or GPU and FPGA simulating platforms are among the hot-topics of ACM-SIGSIM, and have been heavily promoted at WSC'16 or ACM-SIGSIM PADS.

TOPICS

High-quality papers in all aspects of simulation during the Design Automation flow are solicited, including (but not restricted to) the following areas:

- Advanced modeling techniques in High-Level Synthesis, and their execution using novel simulation algorithms.
- Simulation of approximate circuits.
- Simulation of hardware-based neural networks.
- Simulation of On-Chip Machine Learning circuits.
- Simulation of Sensor Networks.
- Parallel algorithms and high performance simulation during the synthesis, placement and routing stages.
- GPU, FPGA and hybrid architecture acceleration.
- Simulation based on distributed controllers.
- Process and delay variation modeling and simulation in datapaths.
- Radiation effects simulation in reliable circuits.
- Datapaths based on variable latency blocks simulation.
- Power and energy simulations to evaluate the design automation algorithms.
- Temperature and aging simulations during the design flow.
- MPSoCs and 3D chips simulation during the synthesis, placement and routing stages.
- Simulation during the Design Space Exploration.
- Simulation visualization techniques to help debug designers.



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SUBMISSION GUIDELINES

For submission guidelines go to <http://scs.org/authorskit/>. Papers should be submitted through the following link: <http://www.softconf.com/sim/SCSC17/>.

TECHNICAL PROGRAMME COMMITTEE

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